Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Third Semester

Electronics and Communication Engineering

EC3352 - Digital Systems Design

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Recall duality in Boolean algebra.	RE	1	2
2.	Define "Minterm" and "Maxterm".	RE	1	2
3.	Distinguish between half adder and full adder.	UN	2	2
4.	Identify the function of select inputs of a MUX.	RE	2	2
5.	Define state diagram.	RE	3	2
6.	Differentiate synchronous and asynchronous sequential circuits.	UN	3	2
7.	Classify Asynchronous sequential circuits.	UN	4	2
8.	List the types of hazards.	RE	4	2
9.	Draw the DTL based NAND gate.	RE	5	2
10.	List the applications of PLA.	RE	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Convert (725.25)8 to its decimal, binary and Hexadecimal equivalent.	AP	1	6
		ii	Express f(a,b,c) = a+b'c as sum of minterms and canonical form.	AP	1	7
			Or			
	b		Using K-map method, Reduce the following boolean function F=∑m(0,2,3,6,7) + d(8,10,11,15) and obtain minimal SOP.	AP	1	13
12.	a		Write a brief note on the following combinational circuits: (i) Full adder (ii) Full subtractor	UN	2	13
			Or			
	b		Derive the circuit that implements an 8-to-3 binary encoder with neat diagram.	UN	2	13
13.	a	i	What is Flip flops? Write about the operations of different flip flops.	UN	3	9
		ii	Convert SR flip flop into JK flip flop.	UN	3	4
			Or			
	b		Summarize 4-bit SISO, SIPO, PIPO and PISO shift register and draw its waveforms.	UN	3	13

14.	a	Analyze an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T=1 and C moves from 1 to 0. Otherwise, the output is 0.	AP	4	13
		Or			
	b	Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is one, input X is transferred to Z. When Y is zero, the output does not change for any change in X.	AP	4	13
15.	a	Implement the functions using PAL W=∈m(2,12,13), X=∈m(7,8,9,10,11,12,13,14,15), Y= ∈m(0,2,3,4,5,6,7,8,10,11,15), Z= ∈m(1,2,8,12,13).	EV	5	13
		Or			
	b	Design a BCD to excess-3 code converter and implement using suitable PLA.	EV	5	13

*PART – C (Marks 1*15 = 15)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
16.	a	Analyze state reduction if possible after designing a clocked synchronous sequential logic circuit using JK flip flops for the following state diagram. Use state reduction if possible.	AN	3	15
		Or			
	b	Design a circuit that has no static hazards and implement the boolean function F(A,B,C,D) = Σ (0,2,6,7,8,10,12) using AND, OR logic.	AN	5	15